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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 09/819,339 | 03/28/2001 | Hong Wang | 884.368US1 | 4244 |

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| EXAMINER | |
|---|---|
| TSAI, HENRY | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2183 | 3 |

DATE MAILED: 05/05/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/819,339 | WANG ET AL. | |
| | Examiner | Art Unit | |
| | Henry W.H. Tsai | 2183 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *3/28/01* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,12-15,16,23 and 24* is/are rejected.

7)☒ Claim(s) *3-11,17-22 and 25-30* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *2* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

**DETAILED ACTION**

***Claim Rejections - 35 USC § 102***

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

2. Claims 1, 2, 15, 16, 23, and 24 are rejected under 35 U.S.C. 102(a) as being anticipated by Rau et al., "Code Generation Schema for Modulo Scheduled Loop", the 25th annual international symposium on microarchitecture, Vol. 23 (1) (2), pp 158-169, December 1992, (in the IDS mailed 3/28/01) hereafter referred to as Rau et al.

Referring to claims 1 and 23, Rau et al. discloses as claimed a processor comprising: an apparatus to rotate registers (see page 161, section 2.1, regarding "a rotating register file is addresses by adding the instruction's register specification field to the contents of the Iteration Control Pointer (ICP) modulo the number of registers in the rotating register file")

in software pipelined loops; and a register rotation prediction unit (this is inherently existing in the Rau et al.'s system in order to execute predicated and speculative executions and Loop Control Operations, as shown in Secs. 2.2-2.4 on page 161, see also Sec. 3.4 on page 164) to predict register addresses for future loop iterations (see Loop Control Operations, as shown in Sec. 2.4 on page 161).

As to claim 2, Rau et al. also discloses: a buffer to hold buffered instructions with predicted register addresses (this is inherently existing in the Rau et al.'s system in order to execute predicated execution as shown in Sec. 2.2 on page 161, see also Sec. 3.4 on page 164).

Referring to claim 15, Rau et al. discloses as claimed a processing system comprising: an execution pipeline (see Sec. 1.1 on page 158, regarding software pipelining); memory (inherently existing in the Rau et al.'s system, such as main memory) coupled to the execution pipeline to hold processor instructions arranged in a software loop (see Loop Control Operations, as shown in Sec. 2.4 on page 161); and register rotation prediction hardware (this is inherently existing in the Rau et al.'s system in order to execute predicated and

speculative executions and Loop Control Operations, as shown in Secs. 2.2-2.4 on page 161, see also Sec. 3.4 on page 164) to predict physical register values for the processor instructions in future iterations of the software loop (see Loop Control Operations, as shown in Sec. 2.4 on page 161).

As to claim 16, Rau et al. also discloses: a software pipeline instruction buffer (this is inherently existing in the Rau et al.'s system in order to execute predicated and speculative executions and Loop Control Operations, as shown in Secs. 2.2-2.4 on page 161, see also Sec. 3.4 on page 164 and Fig. 10(a)) coupled between the execution pipeline and the register rotation prediction hardware to hold the processor instructions in future iterations of the software loop (see Loop Control Operations, as shown in Sec. 2.4 on page 161).

As to claim 24, Rau et al. also discloses: the software pipelined loop comprises at least one branch instruction, the method further comprising, issuing at least one non branch instruction simultaneously with the at least one branch instruction (see Figs. 7 and 8, showing the at least one non branch instruction simultaneously with the at least one branch instruction in the Rau et al.'s system)

***Claim Rejections - 35 USC § 103***

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 12-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rau et al. in view of D'Sa et al. (U.S. Patent No. 6,151,671) hereafter referred to as D'Sa et al.'671.

Rau et al. discloses the claimed invention except for: a trace cache; the trace being configured to hold a prediction hint for each trace; and a trace cache fill unit to apply register rotation prediction to traces as traces are constructed.

D'Sa et al.'671 discloses a system comprising: a trace cache (TC 130, see Fig. 1b); the trace being configured to hold a prediction hint for each trace (see Col. 6, lines 49-61, regarding trace cache 130 storing the branch prediction); and a trace cache fill unit (see Col. 6, lines 49-53, regarding

instruction fetch unit 110 is acting as the instruction source while trace cache unit 130 is in "build mode") to apply register rotation prediction to traces as traces are constructed.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Rau et al.'s system to comprise a trace cache; the trace being configured to hold a prediction hint for each trace; and a trace cache fill unit to apply register rotation prediction to traces as traces are constructed, as taught by D'Sa et al.'671, in order to facilitate the branch prediction and speculative execution for the Rau et al.'s system.

***Allowable Subject Matter***

5. Claims 3-11, 17-22, and 25-30 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

***Conclusion***

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure wherein Rogers et

al.'016 discloses a multi-threaded processor comprising trace cache 62 and trace BTB for the speculative execution; Miller'822 discloses a block oriented cache 44 and reorder buffer 32 similar to a trace cache; and Janik et al.'805 discloses a circular counterflow pipeline processor comprising ROB 16 and branch prediction unit 22 to facilitate branch prediction and speculation for the loop as the claimed invention.

***Contact Information***

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dr. Henry Tsai whose telephone number is (703) 308-7600. The examiner can normally be reached on Monday-Thursday from 8:00 AM to 5:00 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner supervisor, Eddie Chan, can be reached on (703) 305-9712. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the **TC 2100 receptionist whose telephone number is (703) 305-3900.**

8. In order to reduce pendency and avoid potential delays, Group 2100 is encouraging FAXing of responses to Office actions directly into **the Group at fax number:** 703-872-9306.

This practice may be used for filing papers not requiring a fee. It may also be used for filing papers which require a fee by applicants who authorize charges to a PTO deposit account. Please identify the examiner and art unit at the top of your cover sheet. Papers submitted via FAX into Group 2100 will be promptly forward to the examiner.

HENRY W. H. TSAI
PRIMARY EXAMINER
May 3, 2004